

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
JS		6,258,634	07/10/2001	Wang et al.			
		5,910,874	06/08/1999	Iniewski et al.			
		5,646,808	07/08/1997	Nakayama			
		5,519,242	05/21/1996	Avery			
		5,631,793	05/20/1997	Ker et al.			
		5,811,857	09/22/1998	Assaderaghi et al.			
		5,502,328	03/26/96	Chen et al.			
		5,581,104	12/03/96	Lowrey et al.			
JS		5,990,520	11/23/99	Noorlag et al.			
FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
JS	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
JS	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner	JS	Date Considered	5-11-5
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		
Form PTO 1449		Patent and Trademark Office - U.S. Department of Commerce	

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
	5,907,462	05/25/99	Chatterjee et al.			
	5,932,918	08/03/99	Krakauer			
	6,015,992	01/18/00	Chatterjee et al.			
	5,453,384	09/26/95	Chatterjee			

FOREIGN PATENT DOCUMENTS						
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	N. K. Verghese and D. Allstot, "Verification of RF and Mixed-Signed Integrated Circuits for Substrate Coupling Effects", in <i>Proc. of IEEE Custom Integrated Circuits Conf.</i> , 1997, pp. 363-370
	M.Xu, D. Su, D. Shaeffer, T.Lee, and B. Wooley, "Measuring and Modeling the Effects of Substrate Noise on LNA for a CMOS GPS Receiver", <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 473-485, 2001.
	R. Gharpurey, "A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits," in <i>Proc. of IEEE Custom Integrated Circuits Conf.</i> , 1999, pp. 487-490.
	M. Nagata, J. Nagai, K. Hijikata, T. Morie, and A. Iwata, "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits", <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 539-549, 2001.
	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin With Very Low Input Capacitance for High-Frequency or Current-Mode Applications", <i>IEEE Journal of Solid-State Circuits</i> , vol. 35, pp. 1194-1199, 2000.
	M.-D. Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuit for Submicron CMOS VLSI", <i>IEEE Trans. on Electron Devices</i> , vol. 46, pp. 173-183, 1999

Examiner		Date Considered	5-11-5
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		
Form PTO 1449		Patent and Trademark Office - U.S. Department of Commerce	

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

--

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
JY		6,081,002	06/27/2000	Amerasekera et al			
		5,754,381	05/19/1998	Ker			
		5,465,189	11/07/1995	Polgreen et al.			
		5,225,702	07/06/1993	Chatterjee			
		5,012,317	04/30/1991	Rountre			
JY		4,939,616	07/03/1990	Rountree			

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
JY	C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on Different ESD Protection Strategies Devoted to 3.3V RF Applications (2 GHz) in a 0.18µm CMOS Process," in Proc. of EOS/ESD Symp., 200, pp. 251-259.
JY	T.-Y. Chen and M.-D. Ker, "Design on ESD Protection Circuit With Low and Constant Input Capacitance," in Proc. of IEEE Int. Symp. on Quality Electronic Design, 2001, pp. 247-247.
JY	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin With Very Low Input Capacitance for RF or Current-Mode Applications," IEEE Journal of Solid-State Circuits, Vol. 35, pp. 1194-1199, 2000.
Examiner	JY
Date Considered	5-11-5
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449 Patent and Trademark Office - U.S. Department of Commerce	

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
JY	5,629,544	05/13/97	Voldman et al.			
	6,034,397	03/07/00	Voldman			
	5,940,258	08/17/99	Duvvury			
	5,807,791	09/15/98	Bertin et al			
	5,719,737	02/17/98	Maloney			
JY	5,654,862	08/05/97	Worley et al.			

FOREIGN PATENT DOCUMENTS						
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
JY	S.Voldman, et al., "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon- Bound Source/Drain Diodes for ESD Networks," in Proc. of EOS/ESD Symp., 1998, pp. 151-160
	S. Voldman, et al., "Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors," in Proc. of EOS/ESD symposium, 1995, pp. 43-61.
	M.J. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol.30, no. 7, pp.823-825, July 1995.
	G.P. Singh, et al., "High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol.34, no. 11, pp. 1512-1525, Nov. 1999.
JY	H. Sanchez, et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in 02. - $\mu$ m, 3.5-nm Tox, 1.8 -V CMOS Technology, " IEEE Journal of Solid-State Circuits, vol.34 no. 11.pp. 1501-1511, Nov. 1999

Examiner	<i>[Signature]</i>	Date Considered	5-11-5
*Examiner:	Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.		
Form PTO 1449		Patent and Trademark Office - U.S. Department of Commerce	

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

## U.S. PATENT DOCUMENTS

Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
	6,258,634	07/10/2001	Wang et al.			
	5,910,874	06/08/1999	Iniewski et al.			
	5,646,808	07/08/1997	Nakayama			
	5,519,242	05/21/1996	Avery			
	5,631,793	05/20/1997	Ker et al.			
	5,811,857	09/22/1998	Assaderaghi et al.			
	5,502,328	03/26/96	Chen et al.			
	5,581,104	12/03/96	Lowrey et al.			
	5,990,520	11/23/99	Noorlag et al.			

## FOREIGN PATENT DOCUMENTS

Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

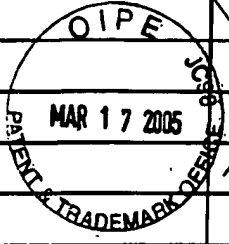
## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	M-D. KER, et al., "CMOS On-Chip ESD Protection Design with Substrate-triggering Technique," Proc. of ICECS, Vol. 1, pp. 273-276, 1998
	C. Duvvury et al., "Dynamic Gate Coupling for NMOS for Efficient Output ESD Protection", Proc. of IRPS, pp. 141-150, 1992

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS							
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate	
	5,907,462	05/25/99	Chatterjee et al.				
	5,932,918	08/03/99	Krakauer				
	6,015,992	01/18/00	Chatterjee et al.				
	5,453,384	09/26/95	Chatterjee				

FOREIGN PATENT DOCUMENTS							
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No	

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	N. K. Verghese and D. Allstot, "Verification of RF and Mixed-Signed Integrated Circuits for Substrate Coupling Effects" in <i>Proc. of IEEE Custom Integrated Circuits Conf.</i> , 1997, pp. 363-370
	M. Xu, D. Su, D. Shaeffer, T. Lee, and B. Wooley, "Measuring and Modeling the Effects of Substrate Noise on LNA for a CMOS GPS Receiver," <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 473-485, 2001.
	R. Gharpurey, "A Methodology for Measurement and Characterization of Substrate Noise in High Frequency Circuits," in <i>Proc. of IEEE Custom Integrated Circuits Conf.</i> , 1999, pp. 487-490.
	M. Nagata, J. Nagai, K. Hijikata, T. Morie, and A. Iwata, "Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits," <i>IEEE Journal of Solid-State Circuits</i> , vol. 36, pp. 539-549, 2001.
	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin With Very Low Input Capacitance for High-Frequency or Current-Mode Applications," <i>IEEE Journal of Solid-State Circuits</i> , vol. 35, pp. 1194-1199, 2000.
	M.-D. Ker, "Whole-Chip ESD Protection Design with Efficient VDD-to-VSS ESD Clamp Circuit for Submicron CMOS VLSI," <i>IEEE Trans. on Electron Devices</i> , vol. 46, pp. 173-183, 1999

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MREP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449 Patent and Trademark Office - U.S. Department of Commerce	

# INFORMATION DISCLOSURE CITATION

OMB No. 0651-0011

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

--	--	--	--

U.S. PATENT DOCUMENTS						
Examiner Initial	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
	6,081,002	06/27/2000	Amerasekera et al			
	5,754,381	05/19/1998	Ker			
	5,465,189	11/07/1995	Polgreen et al.			
	5,225,782	07/06/1993	Chatterjee			
	5,012,317	04/30/1991	Rountree			
	4,939,616	07/03/1990	Rountree			

FOREIGN PATENT DOCUMENTS						
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	C. Richier, P. Salome, G. Mabboux, I. Zaza, A. Juge, and P. Mortini, "Investigation on Different ESD Protection Strategies Devoted to 3.3V RF Applications (2 GHz) in a 0.18µm CMOS Process," in <i>Proc. of EOS/ESD Symp.</i> , 200, pp. 251-259.
	T.-Y. Chen and M.-D. Ker, "Design on ESD Protection Circuit With Low and Constant Input Capacitance," in <i>Proc. of IEEE Int. Symp. on Quality Electronic Design</i> , 2001, pp. 247-247.
	M.-D. Ker, T.-Y. Chen, C.-Y. Wu, and H.-H. Chang, "ESD Protection Design on Analog Pin With Very Low Input Capacitance for RF or Current-Mode Applications," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 35, pp. 1194-1199, 2000.

Examiner	Date Considered
<p>*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	

## INFORMATION DISCLOSURE CITATION

Atty. Docket No.	06720.0086-01	Serial No.	TO BE ASSIGNED
Applicant	Chyh-Yih CHANG		
Filing Date	September 25, 2003	Group:	TO BE ASSIGNED

U.S. PATENT DOCUMENTS						
Examiner Initial*	Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate
	5,629,544	05/13/97	Voldman et al.			
	6,034,397	03/07/00	Voldman			
	5,940,258	08/17/99	Duvvury			
	5,807,791	09/15/98	Bertin et al			
	5,719,737	02/17/98	Maloney			
	5,654,862	08/05/97	Worley et al.			

FOREIGN PATENT DOCUMENTS						
	Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	S.Voldman, et al., "Semiconductor Process and Structural Optimization of Shallow Trench Isolation-Defined and Polysilicon-Bound Source/Drain Diodes for ESD Networks," in Proc. of EOS/ESD Symp., 1998, pp. 151-160
	S. Voldman, et al., "Analysis of Snubber-Clamped Diode-String Mixed Voltage Interface ESD Protection Network for Advanced Microprocessors," in Proc. of EOS/ESD symposium, 1995, pp. 43-61.
	M.J. Pelgrom, et al., "A 3/5 V Compatible I/O Buffer," IEEE Journal of Solid-State Circuits, vol.30, no. 7, pp.823-825, July 1995.
	G.P. Singh, et al., "High-Voltage-Tolerant I/O Buffers with Low-Voltage CMOS Process," IEEE Journal of Solid-State Circuits, vol.34, no. 11, pp. 1512-1525, Nov. 1999.
	H. Sanchez, et al., "A Versatile 3.3/2.5/1.8-V CMOS I/O Driver Built in 02. - $\mu$ m, 3.5-nm Tox, 1.8 -V CMOS Technology," IEEE Journal of Solid-State Circuits, vol.34 no. 11, pp. 1501-1511, Nov. 1999

Examiner	Date Considered
<p>*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</p>	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce